### Low Power VLSI

1. **Course Title**: Low Power VLSI

2. **Credit Structure**
   - Lecture hours per week: 2
   - Tutorial hours per week: 0
   - Practical hours per week: 2
   - Total Credits: 3

3. **Course Code**: EL519

4. **Program/Semester**: M.Tech - Semester III

5. **Category**: Core / **Group core** / Technical Elective / Open Elective / Science Elective

6. **Prerequisite courses**: EL322, EL511

7. **Foundation for**: Masters Project or project based study

8. **Abstract Content**
   - The aim of this 14-15 week course is to give a broad grounding in the principles and practice of Electronic Design Automation techniques for System on Chip Design.
   - The course covers topics in Ultra Low Power VLSI digital circuits (Digital IC design, layout, simulation, synthesis, VLSI design techniques and system architecture; CAD tools and techniques, Low Power, ultra low power circuit techniques and energy harvesting electronics).
   - The course prerequisites are an undergraduate level electronic circuit design course.
   - This course is a design intensive course that will cover moderate to advanced use of the following tools and languages:
     - Magic or Cadence icfb, h/p/lt Spice
     - VHDL simulator, synthesis tool
     - (Circuits) MOS gate characteristics
     - (HDL) VHDL or Verilog
     - CMOS technology (0.18µ CMOS).
   - Individual research survey paper and two significant design project (in teams of two) are assigned during the semester.

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**Optional**

**Suggested Textbook(s)**

- Low Power Design Essentials Jan Rabaey, Springer ©2009
<table>
<thead>
<tr>
<th>Topic Name</th>
<th>Content (2 -3 lines per 4 – 6 lectures)</th>
<th>No. of lectures</th>
</tr>
</thead>
<tbody>
<tr>
<td>Introduction to Low Power IC design and CAD Flows</td>
<td>Early Computers, The first electronic watch, Low power design techniques; Cadence IC front-end back-end tools and flows.</td>
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<td>CMOS Fundamentals</td>
<td>Static CMOS, Dynamic CMOS, Power Delay product, Capacitive and Resistive parasitic.</td>
<td>4</td>
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<td>Deep Submicron issues</td>
<td>Switching current, design of metric for performance, application to standard cell library and low power library</td>
<td>3</td>
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<tr>
<td>Low Power Arithmetic Circuits</td>
<td>Designing combinational circuits, sequential circuits, power consumption in CMOS gates.</td>
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<tr>
<td>Low Power Circuits, Power Reduction Techniques</td>
<td>Low power arithmetic building blocks, leakage components of MOSFET devices and power reduction techniques at circuit, architectural and system level</td>
<td>6</td>
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<tr>
<td>Ultra/ Low Power IC design</td>
<td>Sub-threshold Design technique: Ultimate ultra low power methodology?</td>
<td>2</td>
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<td>Energy Harvesting Electronics</td>
<td>Micro power generation from everyday activities for mobile computing</td>
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<td>Outcomes and Objectives</td>
<td>□ Having successfully completed the module, the student will be able to design and implement CMOS digital circuits and optimize them with respect to size (area), speed and <strong>power dissipation</strong>.</td>
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<td>□ Knowledge and Understanding</td>
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<td>Having successfully completed the module, you will be able to demonstrate knowledge and understanding of:</td>
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<td></td>
<td>1. Introduction to Cadence, Schematic Design, Analogue Layout and Simulation, Extraction and LVS</td>
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<td>2. Digital Simulation and RTL Synthesis</td>
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<td>3. Automatic Place and Route, Pad Rings And Chip Architecture</td>
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<td>4. Low Power System Architecture</td>
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|                                                     | □ Intellectual Skills: Having successfully completed the module, you
will be able to:

1. Advanced IC Design Skills
2. Use of EDA Tools
3. Understanding of Analog Simulation
4. Understanding of Digital Simulation
5. Place and Routing
6. Power Reduction techniques at Circuit, Architectural and System level

☐ Practical Skills:

Having successfully completed the module, you will be able to:

1. Complete skill set for Cadence IC design flow
2. Modelsim simulation and analysis
3. Synthesis Tool

Comments ☐ 100% course work