EL504 Selected Topics in VLSI

Credit Structure
3-0-2-4

Prerequisite courses
Basics of VLSI, Basics of Programming

Course Content

Physical Design and Verification

Physical verification is a process whereby an integrated circuit layout (IC layout) design is verified via EDA software tools to ensure correct electrical and logical functionality and manufacturability.

1. Introduction to PD flow, Floor plan, Power plan
2. Placement, Types of Placement, Congestion
3. Clock tree synthesis, Clock skew, Clock tree optimization
4. Routing, Types of routing, Crosstalk
5. Physical Verification, Timing fixes
6. Project

SystemVerilog Based Verification

SystemVerilog is a hardware description and hardware verification language used to model, design, simulate, test and implement electronic systems. SystemVerilog is based on Verilog and some extensions, and since 2008 Verilog is now part of the same IEEE standard. It is commonly used in the semiconductor and electronic design industry as an evolution of Verilog.

1. Verilog for design and Verification refresh, Introduction to HVLs, Why System Verilog?
2. SystemVerilog Data types
3. Arrays, Queues, OOPs concepts, Classes
4. Randomization, Constraints, Mailboxes, Semaphores, Interfaces, mod port, clocking block
5. BFM development, Code Coverage and functional coverage, Introduction to SV assertions, Demonstration of Memory Test bench using SystemVerilog
6. Project

Grading:

Project 1: 30 %
Project 2: 30 %
Exam (Final): 40 %

Mechanisms/modalities for lecture delivery:

I am comfortable with GMeet or any other platform for lecture delivery. In addition, I create WhatsApp for my every course so that students can reach me any time.

Labs: We will use Cadence Tools through VPN.