Course: IT 209 (Computer Organization)

Note: This would be a first trial of teaching this course completely online. The course content and marks distribution may change. Students will be made aware of the change.

Textbook:

1. ARM Assembly Language: Fundamentals and Techniques by William Hohl, (AAL)
2. Computer Organization and Design: The hardware/software Interface (ARM edition) by John L Hennessy & David A Patterson (This book will be referred to as COD)
3. Computer Architecture: A Quantitative Approach, 5th Edition By John L Hennessy & David A Patterson (you may use earlier editions. It may have different Chapter numbers) (CAQA)

IMPORTANT NOTE: Lecture slides are for my convenience. It may not contain all the topics which I discuss in the class. You are supposed to attend the classes regularly and not depend upon the lecture slides

Course Philosophy: This is an introductory course to the computer organization. It will build on the foundation laid out by the Digital Logic Design (DLD) course. In this course, you will learn about the computer architecture which contains Instruction Set Architecture (ISA), interrupt model, register sets and memory organization. Later on, you will study about the details of the implementation details.

For lab part, you will be working with keil compiler to learn assembly language programming in ARM v4T.

Course Outline:

ARM Architecture (AAL): Chapters 2, 3, 4, 5, 6, 7, 8, 10, 11, 14

Chapter 4 (COD): The Processor
4.1 Introduction
4.2 Logic Design Convention
4.3 Building a Datapath
4.4, 4.5 An overview of Pipelining
4.6 Pipelined Datapath and Control
4.7 Data dependency and hazard
4.8 Control hazard and Structural Hazard
4.9 Exceptions

Chapter 1 (CAQA)
1.1/.2/.3 Defining Computer Architecture
1.4 Trends in technology
1.8 Measuring, reporting and summarizing performance

Chapter 3 (CAQA)
3.1 Instruction Level Parallelism (ILP) Concepts and Challenges
3.2 Basic compiler techniques for exposing ILP
3.3 Reducing Branch costs with advanced branch prediction techniques
3.4 Overcoming Data hazards with dynamic scheduling
3.5 Dynamic scheduling: examples
3.6 Hardware based speculation
3.7 Exploiting ILP using multiple Issue and static scheduling (Super-scalar)
3.8 ILP using dynamic scheduling, multiple issue and speculation
3.9 Limitations of ILP

Appendix B (CAQA) Review of Memory Hierarchy
B.1 Introduction
B.2 Cache performance
B.3 Six basic cache optimization

Grading Policy
Midterm 1: 30%
Midterm 2: 30%
Final exam: 40%
Plagiarism Policy: Students are not allowed to copy HW, Labwork, Quiz or represent someone’s work as their own. Same is true for copying in the exams. Anyone caught cheating (and a person or persons helping him/her to cheat) will get penalty of a full grade (A A to BB or AB to BC etc). This rule will be strictly enforced.