EL427 Testing of VLSI Circuits (3-0-0-3)
MTech SEM III / BTech SEM VII

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Prerequisites: Knowledge of VLSI systems

Abstract Content:
Introduction to VLSI testing: test process and automatic test equipment, test economics and product quality, test economics.
Physical faults and their modeling. Fault equivalence and dominance; fault collapsing.
Fault simulation: parallel, deductive and concurrent techniques; critical path tracing.
Test generation for combinational circuits: Boolean difference, D-algorithm, Podem, etc.
Exhaustive, random and weighted test pattern generation; aliasing and its effect on fault coverage.
Test pattern generation for sequential circuits.
Design-for-Testability: ad-hoc and structures techniques, scan path and LSSD, Full, partial, Random-Access scan.

Optional: Verification of Circuit, Formal verification, simulation based verification, Hardware Emulation Based Verification.

Suggested Texts:

Evaluation:
1) 1ST In-Sem – 15%
2) 2nd In-Seem – 15%
3) End-Sem Exam – 50%
4) Term paper presentation, attendance etc. – 10%
5) Course project –10%

Class attendance is compulsory. There will be no unannounced quizzes