Abstract – This is an introductory course on VLSI Design, which will enable the students to understand the fundamentals of the CMOS technology, including: trends in the semiconductor industry – Moore’s Law and Scaling, CMOS fabrication/processing steps, MOS devices and characteristics, building circuits and gates with MOSFETS, estimating the performance and price of CMOS circuits, designing combinational and sequential CMOS circuits, CMOS array structures, etc.

Tentative Syllabus

1) Introduction
   a) Trends in VLSI/Semiconductor industry, benefits and challenges
   b) ITRS Roadmap, Beyond CMOS, etc

2) Review of semiconductor device fundamentals
   a) Carrier classification: Bonding model, Energy band diagrams, carrier concentrations
   b) M-S and PN junction, and related electrostatics, etc.

3) MOS capacitor and MOS transistor theory
   a) NMOS, PMOS, CMOS inverter – I-V characteristics, etc.

4) CMOS fabrication technology – Process Sequence, Layout Rules, etc

5) CMOS circuit characterization and Performance/Price estimation
   a) RC delay models, Parasitic delays, logical/stage/electrical effort and related transistor sizing
   b) Static/Dynamic Power dissipation
   c) Interconnects and wires
      i) Resistance, capacitance,
      ii) Delay
   d) Transistor and interconnect scaling – Scaling rules

6) Combinational circuit design
   a) Static CMOS, standard gates, compound gates, adder circuit
   b) Pseudo NMOS
   c) Dynamic circuits
   d) Pass-transistor circuits, Transmission gates

7) Sequential circuit design
   a) Latch, and Flip-flop,
   b) Sequencing methods
      i) Setup and hold time constraints, effect of clock-skew
   c) FSM examples

8) Array Subsystems
   a) SRAM
   b) PLA, ROM, etc
   c) Emerging array structures – hybrid nanoelectronics - CMOL

9) Fundamentals of testing
   a) Fault models – stuck-at faults, etc.
   b) Observability and controllability

** As suggested by the VLSI Faculty Group, Topic Nos. 8, and 9 may be replaced with topics in Verilog:
   Verilog codes for combinational and sequential circuits, such as: Decoders, Encoders, MUX, De-MUX, Comparators, FSM, ALU, registers, etc.
Grading Policy:
1) InSem Exam-1: 30%
2) InSem Exam-2: 30%
3) Quiz and/or Homeworks$: 5%
4) Final Exam: 35%

Total: 100%

$: Practice homeworks may be given. These may involve assignments that require the use of Circuit Simulation tools, and use of MATLAB®

Books:
Text book:
(1) CMOS VLSI Design: A circuits and systems perspective; by Weste, Harris, Banerjee 621.395 WES #022635

Reference books:
(1) CMOS Digital Integrated circuits; by Kang & Leblebici 621.395 KAN #020053
(2) Semiconductor Device Fundamentals, by Pierret 621.38152 PIE #021544
(3) Digital integrated circuits : a design perspective, 2nd ed; by Rabae et al. 621.395 RAB
(4) Essentials of Electronic Testing; by Bushnell, and Agarwal 621.395 BUS #023320