EL114 Digital Logic Design (3-0-3-4.5)

Tentative Syllabus

Number Systems Representations: Signed 2's Complement, Signed 1's Complement, Signed Magnitude, BCD, etc

Boolean Algebra: Axioms and theorems, DeMorgan, Duality, Expression manipulation using axioms and theorems.


Sequential Logic: Simple circuits with feedback, Basic latches, Clocks, R-S latch, Master-slave latch, J-K flip-flop, T flip-flop, D flip-flop, Storage registers, Shift registers, Ripple counters, Synchronous counters, Finite state machine (Moore / Mealy machine), FSM with single/multiple inputs and single/multiple outputs, etc.

Hardware Description Language: Verilog programming and simulation, Structural specification, Behavioural specification, Dataflow Modeling, Testbench, Testing using test vectors, Testing using waveforms, Design basic blocks and use them to build larger circuits, Case studies, adders, ALU, Counters, Shift-registers, Register bank, FSM design example, etc.

Introduction to CMOS logic design: MOSFET and its operation, building MOSFET based logic gates, and simulation using LTSpice.

Books


Evaluation Method (tentative)

1st In-Semester Examination: 20%
2nd In-Semester Examination: 20%
Labs (including attendance and performance in lab): 30%
End-Semester Examination: 25%
Other (Quiz (indirect-attendance) etc): 5%
Total: 100%
Attendance Policy:

- Attendance in Lecture: Not compulsory. However, the instructor can take surprise quizzes, which will indirectly reflect your attendance.
- Attendance in Labs: Compulsory. A student may be permitted to remain absent from a specific lab, only if prior notification is given, and an approval is granted from the instructor. The lab attendance over the semester should be above 80%.