EL-520    Digital System Design using Verilog

Credit Structure (L-T-P-Cr): 3-0-2-4        Semester: Winter 2017


Course Objectives:

- Learn the hierarchy and design methodology in digital and VLSI systems.
- Analyze the importance and applicability of Hardware Description Language (HDL).
- Learn basics of Computer-Aided Design (CAD) using Verilog Electronic Design Automation (EDA) tool by theoretical as well as practical exercises.
- Conceptual learning of logic synthesis, delay, test benches, timing checks, memory, state machines using Verilog.

Course Contents:

1) Introduction
   a) Hierarchical and design methodology in digital and VLSI systems
   b) HDL language and Verilog EDA tool
2) Description of modules, nets, operators and parameters in Verilog
3) Verilog module and implementation schemes
   a) Gate level modeling
   b) Data flow modeling
   c) Behavioral level modeling
4) Designing and implementation of Combinational circuits
   a) Basic logic gates
   b) Half adder, full adder, Multiplexers, etc.
   c) Test benches
5) Sequential circuits implementation using Verilog
   a) Latch, flip-flops
   b) Synchronous and asynchronous operation
   c) Registers, Counters
6) Delay
7) Task, Function, Memories, Stack, Queue
8) FSM Synthesis
   a) Mealy
   b) Moore
9) File input/output

Reference Books:


Course Evaluation Policy:

I In-Semester Examination: 15%
II In-Semester Examination: 15%
End-Semester Examination: 25%
Labs: 25%
Project*: 10%
Others (Quiz, Attendance): 10%
Total: 100%

* Project shall comprise of a few assignments, logic designs implementation using Verilog and/or paper presentation/writing.