EL424: Laboratory in VLSI

Lectures: Every Mon, 0930-1025, CEP 202
Labs: Every Wed, 1400-1800, Lab 205

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Course Description: The motivation for the course is to emphasize more on the practical aspect of VLSI design by using the concepts already taught in previous VLSI courses.

Prerequisite(s): Digital System Architecture, Introduction to VLSI.

Credit Hours: 1-0-4-3

Text(s): Handouts, Tutorials, Papers, Internet and Digital Integrated Circuits, 2nd Edition (Rabaey, Chandrakasan and Nikolic);

Distribution:
Coursework – 100%.
A Description of the grading process is discussed in the accompanying document.

Grade Distribution:
Assignment 1  20%
Assignment 2  20%
Assignment 3  40%
Assignment 4  20%

Grading:
Course Objectives:
At the completion of this course, students will be able to:

1. Design and implement CMOS analog and digital circuits
2. Analyze circuits in Spice, C and matlab
3. Use specific technology library files
4. appreciate the use of simulation tools in spice, matlab and cadence for design decisions

Knowledge and Understanding:
Having successfully completed the module, you will be able to demonstrate knowledge and understanding of:

1. Cadence icfb, schematic Design
2. Digital Simulation in modelsim
3. Device/circuit simulations in spice

Intellectual Skills:
Having successfully completed the module, you will be able to:

1. Understanding and preparing datasheets
2. EDA tools
3. Understanding of Digital and Analog Simulation

Extra Help: Do not hesitate to come to my office during office hours or by appointment to discuss a homework problem or any aspect of the course.

Attendance Policy: Students are responsible for all missed work, regardless of the reason for absence. It is also the absentee’s responsibility to get all missing notes or materials.

Important Dates:

Assign 1 Assignment Given/ Handin Date ............ Aug 04/Aug 19
Assign 2 Assignment Given/ Handin Date ............ Aug 25/Sep 08
Assign 3 Assignment Given/ Handin Date ............ Sep 08/Sep 29
Assign 4 Assignment Given/ Handin Date ............ Sep 29/Late Oct
**Tentative Course Outline:**
The weekly coverage might change as it depends on the progress of the class. However, you must keep up with the reading assignments if given.

<table>
<thead>
<tr>
<th>Week</th>
<th>Content</th>
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| Week 1  | • Introduction to Course  
          • Reading assignment: CMOS fundamentals                             |
| Week 2  | • Spice Simulation  
          • Reading assignment: Spice, Filters                                 |
| Week 3  | • VHDL Basics  
          • Reading assignment: VHDL                                             |
| Week 4  | • VHDL to Hardware  
          • Reading assignment: VHDL                                             |
| Week 5  | • Hardware to VHDL  
          • Reading assignment: VHDL                                             |
| Week 6  | • VHDL Advanced                                                       |
| Week 7  | • VHDL Advanced                                                       |
| Week 8  | • Cadence ICFB                                                        |
| Week 9  | • Simulation                                                          |
| Week 10 | • Circuit Design                                                       |
| Week 11 | • Layout                                                               |
| Week 12 | • Extracted View and Simulation                                       |
| Week 13 | • System/Architectural Level Considerations                           |
| Week 14 | • Discussions                                                          |