Load Modelsim

CAD->Modelsim

IMPORTANT Information!

The 6.1 release will use the following licensing versions: FLEXlm v9.5; Mentor Graphics Licensing MGLS v2004.2 and FCLS 2004.328.

- **Key Information**
  - ModelSim platform changes

- **Product Changes**
  - Changes in ModelSim functionality

- **New Features**
  - The latest ModelSim features
Load Modelsim
CAD->Modelsim

Click this and get rid of it
Libraries
Transcript -> commands
Usual Windows Style menus
Step 1: Create a Project

- File -> New -> project
Create the new directory
Add the files
Add the files

• You can reference the files, or you can copy into the directory – this is a good idea if you are going to modify things
Note the transcript & workspace...
How to add more files

- File -> Add to project -> Existing Files
Now we have the complete project
Note the status and type
How to edit properties?

- Right click on VHDL filename
- Choose properties from the popup menu
  - Can change VHDL settings
What Now – Compile

• We can compile individual files
  – Useful for large designs

• We can compile ALL the VHDL files
  – What we usually do when all the individual files have been checked

• Compile -> Compile All (from the menus)
  – Or use the menu bar icon
Compile Status
What if it goes wrong?

- E.g. syntax error
Edit a VHDL File

• Double click on the VHDL file to bring up the editor
• Double click on the error in the transcript to see where the error is…

Double Click Again
Debug the model
Simulate

• Simulate -> Start Simulation

• Or click on the icon:
List of compiled Units

Look for "work"
That’s your stuff

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>work</td>
<td>Library</td>
<td>H:/vhdl/testcounter/work</td>
</tr>
<tr>
<td>vital2000</td>
<td>Library</td>
<td>$MODEL_TECH/../vital2000</td>
</tr>
<tr>
<td>ieee</td>
<td>Library</td>
<td>$MODEL_TECH/../ieee</td>
</tr>
<tr>
<td>modelsim_lib</td>
<td>Library</td>
<td>$MODEL_TECH/../modelsim_lib</td>
</tr>
<tr>
<td>std</td>
<td>Library</td>
<td>$MODEL_TECH/../std</td>
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<tr>
<td>std_developerskit</td>
<td>Library</td>
<td>$MODEL_TECH/../std_developerskit</td>
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<tr>
<td>synopsys</td>
<td>Library</td>
<td>$MODEL_TECH/../synopsys</td>
</tr>
<tr>
<td>verilog</td>
<td>Library</td>
<td>$MODEL_TECH/../verilog</td>
</tr>
</tbody>
</table>
Choose the test circuit
The Design loads up...
Get wave viewer

• type: at the command line:
  – add wave –r /*

Click Here To Break Off Waveform window
Waveform Window
Run Commands

- run
- continue
- restart
- Run time
Run a 50 us simulation

• Type the following command:
  – run 50 us