Assignment:

Warning: This coursework is intended to be a group work(two). We encourage students to discuss the problems, however, if there is evidence that material has been copied or only slightly altered without being properly referenced the coursework will result in a zero mark.

General Hints: For all simulations include the schematic and the output waveform showing a selection of most relevant signals. The waveforms should look as you would expect them to look like on an oscilloscope. All choices of design or parameters you are making should be justified. All simulation results should be put into context with theoretical analysis followed by a brief discussion.

The design is to be implemented in VHDL and Modelsim. You can also obtain the student version from Modelsim website.

1. In the previous assignment you have designed and simulated a 1 bit adder. Using this, analyse, design and simulate (using structural description in VHDL) an 8 bit array multiplier.

2. Discuss one of the following (with mathematical expression and gate level circuit, delay and area equations, (NO HDL and a maximum 2 page limit)):
   (a) Booth Multiplier (lowest 6 regn ids )
   (b) Baugh-Wooley Multiplier (middle 6 regn ids)
   (c) Pezaris Multiplier (last 5 regn ids)


Maximum 4 page limit.

No makeup quizzes or exams will be given.

Late submission will be penalized by a 5% mark reduction per day.