EL512: Assignment #5

Design and Simulation of Shift Register and an LFSR.

Assignment:

Warning: This coursework is intended to be a group work (two). We encourage students to discuss the problems, however, if there is evidence that material has been copied or only slightly altered without being properly referenced the coursework will result in a zero mark.

General Hints: For all simulations include the schematic and the output waveform showing a selection of most relevant signals. The waveforms should look as you would expect them to look like on an oscilloscope. All choices of design or parameters you are making should be justified. All simulation results should be put into context with theoretical analysis followed by a brief discussion.

The design is to be implemented in VHDL and Modelsim. You can also obtain the student version from Modelsim website.

1. Design, analyse and simulate (using structural description in VHDL) an 1 bit register.

2. Design, analyse and simulate (using structural description in VHDL) an 8 bit shift register from the 1 bit register.

3. Design, analyse and simulate (using structural description in VHDL) an Linear Feedback Shift Register (LFSR) with 4 outputs. State the minimum number of stages so that it can be defined as a random number generator. Discuss the mathematical formulation behind such a random function generator.

Extra credit for those who can come up with a close to ideal random number generator. State whether it is possible or not?

Deadline: 08. Apr. 2016, 5pm.

Maximum 4 page limit.

No makeup quizzes or exams will be given.

Late submission will be penalized by a 5% mark reduction per day.

© Biswajit Mishra 2016