EL519: Assignment #2

Power-Delay Analysis on CMOS Multiplier Circuit.

Assignment:

Warning: This coursework is intended to be a group (consisting of 2 members) work. No plagiarism!

General Hints: For all simulations include the schematic. If appropriate, the circuit netlist or parts of it should be included in the report. All simulation results should be put into context with theoretical calculations followed by a brief discussion. The design is to be implemented in Spice. If the student chose to it in Cadence Virtuoso environment, then inform me.

Exercise:

Consider a single full adder circuit that will be scalable for an array multiplier.

Perform the following steps for the course work:

- Find the delay and power for the adder circuit using 0.18µm CMOS.
- Write a gate level (structural) circuit representation in VHDL for the adder.
- Using this adder - describe a gate level (structural) for an array multiplier.
- Find the delay and Power figure for varying activity factor for the multiplier circuit using the information that you have obtained from circuit simulation.
- Discuss the array multiplication for the signed and unsigned multiplication.
- Discuss any low power technique that can further reduce the power consumption from the circuit.

No makeup quizzes or exams will be given.
Late submission will be penalized by a 5% mark reduction per day.

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