Pipelined Processor: 4 stages, no stack

The Microprogram Memory is organised in 2 parallel blocks, each containing the control codes for one particular pipeline stage, as indicated by the suffixes E and M.

### Fixed-field Instruction Code (4x4 bits):

<table>
<thead>
<tr>
<th>Primary Op Code</th>
<th>R3</th>
<th>R2</th>
<th>R1</th>
</tr>
</thead>
</table>

**R1**: Destination register for MOVE, LOAD and Arithmetic/Logic Instructions.

**R2**: Source register for MOVE, STORE and Arithmetic/Logic instructions; **Condition Code** for BRANCH instruction; **Source address** register for LOAD instruction.

**R3**: Source register for Arithmetic/Logic instructions; **Destination address** register for the STORE instruction, **Branch address** register for Absolute/Direct BRANCH.

**R3R2R1**: 12-bit **Immediate** data; **Displacement** in Program-relative BRANCH.