

Learning Objectives: Hardware Description Language (HDL) based digital design process and rapid prototyping tools like Field Programmable Gate Arrays (FPGA) are becoming ubiquitous components in the design of complex digital systems. Their applications are far reaching – design of processors, filters, networking systems.

This course intends to familiarize the students with Verilog HDL, followed by the considerations needed for implementing HDL designed systems on FPGAs.

Teaching Method: Lectures and Laboratory

Lecture – Three lectures per week of 55 minutes duration each
Laboratory – One lab of two hours each

Evaluation: Continuous evaluation will be carried out. (Lab – 20%, Class Test (two) – 40%, Final Examination – 40%).

Topics:

Lectures

1. Introduction to digital design methodology
2. Fundamentals of sequential logic design – Mealy, Moore machines
3. Timing optimization and clock skew
4. Introduction to logic design with Verilog
5. Computer organization and design

Laboratory topics in addition to design exercises

1. Overview of different Programmable Logic Device (PLD) platforms
2. Components of typical PLD. Embedded memory, PLL
3. Functional simulation of design using on-chip resources
5. Use of vendor provided canned functionality. Example – Xilinx Coregen
6. On-chip verification using PLD software.

Reference Books (In alphabetical order)

Verilog

1. Cilleti – Advanced digital design using Verilog HDL
2. Palnitkar – Verilog HDL

Computer Architecture

3. Patterson, Hennessy – Computer Organization and design – The hardware / software interface
4. Mark Gordon Arnold – Verilog digital computer design

(Some more reference books may be identified as the course progresses)