Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.
DSA Project 2009

Mohit Maheshwari  200601008
Prashant Garg       200601144
4/20/2009
# TABLE OF CONTENTS

1. Problem Statement ......................................................................................................................... 4

2. Functional Specification .................................................................................................................. 4
   2.1 Introduction ................................................................................................................................. 4
   2.2 Objective .................................................................................................................................... 4
   2.3 Approach .................................................................................................................................... 4
   2.4 Block Diagram ............................................................................................................................ 5
      2.4.1 System .................................................................................................................................. 5
      2.4.2 Encoder ............................................................................................................................... 6
      2.4.3 Decoder ............................................................................................................................... 7
   2.5 RTL Model ................................................................................................................................... 8
      2.5.1 Encoder ............................................................................................................................... 8
      2.5.2 Decoder ............................................................................................................................... 10
   2.6 Floor Plan ................................................................................................................................... 12
      2.6.1 Encoder ............................................................................................................................... 12
      2.6.1 Decoder ............................................................................................................................... 12
   2.7 Functional Simulation .................................................................................................................. 13
      2.7.1 Encoder ............................................................................................................................... 13
   3. Reports .......................................................................................................................................... 13
      3.1 Encoder Reports ....................................................................................................................... 13
         3.1.1 HDL Synthesis Report ....................................................................................................... 13
         3.1.2 Device utilization summary ............................................................................................... 14
         3.1.3 Timing Report .................................................................................................................... 14
         3.1.4 Mapping Report ............................................................................................................... 14
         3.1.5 Post Place & Route Report ............................................................................................... 15
      3.2 Decoder Reports ....................................................................................................................... 15
1. PROBLEM STATEMENT

Design and implement a FPGA based IR based encoder and decoder compatible with TSOP38. You can base the encoder design as per the chip HT-12E and decoder as per HT-12D. The datasheets for both are part of projects_2009 folder in the lectures folder. Try and demonstrate the setup using breadboards and FPGA trainer kits. (TSOP, IR encoder documents attached).

2. FUNCTIONAL SPECIFICATION

2.1 INTRODUCTION

Infra red is a widely accepted wireless communication standard for short and medium range communication. It is widely used in remote controls for TV, DVD players, home theaters etc. This project discusses the design and implementation details of Infra red based encoder and decoder compatible with TSOP38. The encoder performs the task of accepting data and address inputs, encoding them and finally transferring it to the Infra-Red transmission circuit. The encoded signals are received by TSOP38 which is connected to the decoder. The decoder then decodes the data, checks if the data is intended for it and displays the data on the FPGA LEDs. The design has been implemented using a self-designed protocol where we have 4-address and 4-data bits which are sent along with a start bit in the beginning. Some of the basic features of the design have been articulated below:

1.) 4-bit address and 4-bit data length
2.) Carrier frequency of 38-Khz as defined by NEC
3.) Control inputs for sending and receiving data
4.) Pulse Width Modulation
5.) Synchronized at both transmitter and receiver
6.) Designed for multiple receivers
7.) Error free output

2.2 OBJECTIVE

To design an FPGA encoder with a control input which encodes the data and address bits (create a packet) and transmits the packet as an IR signal at 38 KHz to the Infra red (IR) LED. The IR LED should pass the encoded signal to the TSOP chip. The TSOP chip must receive the data and then transfer it to the decoder(s). The decoder(s) after performing an address check should display the data on the LEDs of the respective FPGA.

2.3 APPROACH

The protocol defined for the Infra red communication is shown in the figure below. Figure (a) shows the start bit with duration of 4 ms and a duty cycle of 75%. Figure (b) consists of logical ‘1’ and logical ‘0’ each of duration 4ms having duty cycle of 50% and 25% respectively. Figure (c) depicts that when the enable is kept high the packet will be transmitted at every 66ms. The packet is shown in Figure (d). As the duration of a complete packet is 36 ms, the delay of 30 ms occurs between two consecutive packets.
The block diagrams show the basic approach to implement the encoder, decoder and the complete system.

2.4 BLOCK DIAGRAM

2.4.1 SYSTEM
## 2.4.2 ENCODER

![Encoder Diagram]

- **System Clock**
- **Pre-scale Block**
- **Input Address + Data (8-bit)**
- **NEC Signal Encoder**
- **Control Block**
- **Encoded Output for transmission**

**Input [1:8]**

**Enable**

**Output**
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.

2.4.3 DECODER

System Clock

Pre-scale Block

Input Signal Received

Control Block

Input Address Verification

If verified

Data retrieval

Decoded Output (8-bit)
2.5 RTL MODEL

2.5.1 ENCODER
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.
2.5.2 DECODER
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.

2.6 FLOOR PLAN

2.6.1 ENCODER

2.6.1 DECODER
2.7 FUNCTIONAL SIMULATION

2.7.1 ENCODER

<table>
<thead>
<tr>
<th>Now: 1.0001e+08 ns</th>
<th>0 ns</th>
<th>20000040 ns</th>
<th>40000080 ns</th>
<th>60000120 ns</th>
<th>80000160 ns</th>
<th>10000200 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>enq</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>clk</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[101]</td>
<td>186</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r(1)</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r(2)</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r(3)</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r(4)</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r(5)</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r(6)</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r(7)</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>r(8)</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ena</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T/C_FILE[21:0]</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T/C_ERROR[31:0]</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3. REPORTS

3.1 ENCODER REPORTS

3.1.1 HDL SYNTHESIS REPORT

Macro Statistics
# Adders/Subtractors : 3
32-bit adder : 2
32-bit subtractor : 1
# Counters : 2
32-bit up counter : 2
# Registers : 4
1-bit register : 2
32-bit register : 2
# Comparators : 3
33-bit comparator less : 3
# Multiplexers : 3
1-bit 4-to-1 multiplexer : 1
32-bit 4-to-1 multiplexer : 2
3.1.2 DEVICE UTILIZATION SUMMARY

<table>
<thead>
<tr>
<th></th>
<th>Utilized</th>
<th>3584</th>
<th>5%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slices:</td>
<td>204</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of Slice Flip Flops:</td>
<td>130</td>
<td>7168</td>
<td>1%</td>
</tr>
<tr>
<td>Number of 4 input LUTs:</td>
<td>378</td>
<td>7168</td>
<td>5%</td>
</tr>
<tr>
<td>Number of IOs:</td>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of bonded IOBs:</td>
<td>11</td>
<td>141</td>
<td>7%</td>
</tr>
<tr>
<td>Number of GCLKs:</td>
<td>2</td>
<td>8</td>
<td>25%</td>
</tr>
</tbody>
</table>

3.1.3 TIMING REPORT

Clock Information:

<table>
<thead>
<tr>
<th>Clock Signal</th>
<th>Clock buffer(FF name)</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>BUFGP</td>
<td>33</td>
</tr>
<tr>
<td>clk11</td>
<td>BUFG</td>
<td>97</td>
</tr>
</tbody>
</table>

Asynchronous Control Signals Information:
No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4
Minimum period: 17.737ns (Maximum Frequency: 56.380MHz)
Minimum input arrival time before clock: 7.733ns
Maximum output required time after clock: 8.932ns
Maximum combinational path delay: No path found

Timing Detail:
All values displayed in nanoseconds (ns)

Timing constraint: Default period analysis for Clock 'clk'
Clock period: 6.537ns (frequency: 152.979MHz)
Total number of paths / destination ports: 1585 / 66

CPU : 22.67 / 23.22 s | Elapsed : 23.00 / 23.00 s

3.1.4 MAPPING REPORT

Design Summary:

Logic Utilization:

<table>
<thead>
<tr>
<th></th>
<th>Utilized</th>
<th>7,168</th>
<th>1%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Flip Flops:</td>
<td>130</td>
<td>7,168</td>
<td>1%</td>
</tr>
<tr>
<td>Number of 4 input LUTs:</td>
<td>247</td>
<td>7,168</td>
<td>3%</td>
</tr>
</tbody>
</table>

Logic Distribution:

<table>
<thead>
<tr>
<th></th>
<th>Utilized</th>
<th>3,584</th>
<th>5%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of occupied Slices:</td>
<td>199</td>
<td>3,584</td>
<td>5%</td>
</tr>
<tr>
<td>Number of Slices containing only related logic:</td>
<td>199</td>
<td>199</td>
<td>100%</td>
</tr>
<tr>
<td>Number of Slices containing unrelated logic:</td>
<td>0</td>
<td>199</td>
<td>0%</td>
</tr>
</tbody>
</table>
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.

**Total Number 4 input LUTs:**
- Number used as logic: 247 (375 out of 7,168, 5%)
- Number used as a route-thru: 128
- Number of bonded IOBs: 11 out of 141 (7%)
- Number of GCLKs: 2 out of 8 (25%)

Total equivalent gate count for design: 3,695
Additional JTAG gate count for IOBs: 528
Peak Memory Usage: 141 MB

### 3.1.5 POST PLACE & ROUTE REPORT

Device Utilization Summary:
- Number of BUFGMUXs: 2 out of 8 (25%)
- Number of External IOBs: 11 out of 141 (7%)
- Number of LOCed IOBs: 11 out of 11 (100%)
- Number of Slices: 199 out of 3584 (5%)
- Number of SLICEMs: 0 out of 1792 (0%)

### 3.2 DECODER REPORTS

#### 3.2.1 HDL SYNTHESIS REPORT

Macro Statistics
- # ROMs: 1
- 4x32-bit ROM: 1
- # Adders/Subtractors: 4
- 32-bit adder: 4
- # Counters: 2
- 32-bit up counter: 2
- # Registers: 22
- 1-bit register: 17
- 32-bit register: 5
- # Comparators: 7
- 33-bit comparator greater or equal: 1
- 33-bit comparator greater: 3
- 33-bit comparator less: 1
- 33-bit comparator less or equal: 2
- # Multiplexers: 10
- 1-bit 8-to-1 multiplexer: 8
- 32-bit 4-to-1 multiplexer: 2

#### 3.2.2 DEVICE UTILIZATION SUMMARY

- Number of Slices: 250 out of 3584 (6%)
- Number of Slice Flip Flops: 176 out of 7168 (2%)
- Number of 4 input LUTs: 463 out of 7168 (6%)
- Number of IOs: 11
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.

Number of bonded IOBs: 11 out of 141 7%
Number of GCLKs: 2 out of 8 25%

3.2.3 TIMING REPORT

Clock Information:

<table>
<thead>
<tr>
<th>Clock Signal</th>
<th>Clock buffer(FF name)</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>BUFGP</td>
<td>33</td>
</tr>
<tr>
<td>clk11</td>
<td>BUFG</td>
<td>143</td>
</tr>
</tbody>
</table>

Asynchronous Control Signals Information:
No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: 24.192ns (Maximum Frequency: 41.335MHz)
Minimum input arrival time before clock: 17.456ns
Maximum output required time after clock: 7.281ns
Maximum combinational path delay: No path found

Timing Detail:
All values displayed in nanoseconds (ns)

Timing constraint: Default period analysis for Clock ‘clk’
Clock period: 6.537ns (frequency: 152.979MHz)
Total number of paths / destination ports: 1585 / 66

CPU : 24.61 / 25.19 s | Elapsed : 24.00 / 25.00 s

3.2.4 MAPPING REPORT

Design Summary

Logic Utilization:

Number of Slice Flip Flops: 172 out of 7,168 2%
Number of 4 input LUTs: 336 out of 7,168 4%

Logic Distribution:

Number of occupied Slices: 242 out of 3,584 6%
Number of Slices containing only related logic: 242 out of 242 100%
Number of Slices containing unrelated logic: 0 out of 242 0%

Total Number 4 input LUTs:
Number used as logic: 461 out of 7,168 6%
Number used as logic: 336
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.

Number used as a route-thru: 125
Number of bonded IOBs: 11 out of 141 7%
IOB Flip Flops: 4
Number of GCLKs: 2 out of 8 25%

Total equivalent gate count for design: 4,768
Additional JTAG gate count for IOBs: 528
Peak Memory Usage: 142 MB

3.2.5 POST PLACE & ROUTE REPORT

Device Utilization Summary:
Number of BUFGMUXs: 2 out of 8 25%
Number of External IOBs: 11 out of 141 7%
Number of LOCed IOBs: 11 out of 11 100%
Number of Slices: 242 out of 3584 6%
Number of SLICEMs: 0 out of 1792 0%

4. EXPERIMENT

4.1 KIT ARRANGEMENT (1 TRANSMITTER & 2 RECEIVERS)
4.2 TRANSMITTED SIGNAL ON DSO

![Image of transmitted signal on DSO](image1)

4.3 RECEIVED SIGNAL ON DSO

![Image of received signal on DSO](image2)
5. CODE

5.1 ENCODER

// Encoder .v
module iren(in,out,ena, clk);
input[1:8] in;
output out;
input clk;
input ena;
reg clk1=0,clk2=0;
integer i=0,j=0,k=0,m=0,n=0,p=0,x=0, count=0;
reg temp=1;
always @(posedge clk)
beg
if(i == 53)
begin
    clk1 = ~clk1;
i=0;
end
else
i = i+1;
end
always @(posedge clk1)
beg
if (ena == 1)
begin
    if (j== 0 && count == 0)
begin
        if(p < 117)
begin
            temp = 1;
p=p+1;
        end
    else
        begin
            temp=0;
p=p+1;
        end
    end
else
begin
    if(in[j] == 1 && count == 0)
begin
        if(p < 78)
begin
            temp = 1;
p=p+1;
        end
    else
        begin
            temp=0;
p=p+1;
        end
    end
end
end
}
end
else
begin
    temp=0;
p=p+1;
end
end
else if (in[j] == 0 && count == 0)
begin
    if(p < 39)
    begin
        temp = 1;
p=p+1;
    end
else
begin
    temp=0;
p=p+1;
end
end
end
if(p == 156)
begin
    p=0;
j=j+1;
    if(j==9)
    begin
        j=0;
count = 1000;
    end
end
if (count != 0)
begin
    temp=0;
count=count-1;
end
else
begin
temp=0;
end
end

assign out = clk1 && temp;
endmodule

// Encoder .ucf

NET "clk"  LOC = "p76"  ;
NET "ena"  LOC = "p141"  ;
NET "in[1]"  LOC = "p122"  ;
NET "in[2]"  LOC = "p123"  ;
NET "in[3]"  LOC = "p124"  ;
5.2 DECODER

// Decoder .v

module irdec(in, out, clk, ena);

input in;
input clk;
input ena;

output reg [1:8]out = 8'b 00000000;
reg [1:8] temp;
reg clk1=0;
integer i=0,p=0,j=0,a=1;
integer flag=0;
integer flag1=0, count=0;

always @(posedge clk)
begin
    if(i == 53)
        begin
            clk1 = ~clk1;
            i=0;
        end
    else
        i = i+1;
end

always @(posedge clk1)
begin
    if(ena==1)
        begin
            if(in==0)
                begin
                    if(j==0)
                        begin
                            p=0;
                        end
                    else
                        begin
                            j=j+1;
                            p=p+1;
                        end
                end
            else
                begin

```
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.

\[
j = 0;
\]
\[
\text{end}
\]
\[
\text{if}(p>110 \&\& \text{flag1}==0)
\begin{align*}
\text{flag} &= 1; \\
\text{flag1} &= 1; \\
\text{count} &= 0;
\end{align*}
\]
\[
\text{end}
\]
\[
\text{if}(\text{flag} == 1 \&\& \text{count}==156)
\begin{align*}
\text{if}(p>60 \&\& j==0)
\begin{align*}
\text{temp}[a] &= 1; \\
a &= a+1;
\end{align*}
\text{end}
\text{else if } (p<60 \&\& j==0)
\begin{align*}
\text{temp}[a] &= 0; \\
a &= a+1;
\end{align*}
\text{end}
\end{align*}
\]
\[
\text{if}(\text{temp}[1] == 1 \&\& \text{temp}[2] == 1 \&\& \text{temp}[3] == 1 \&\& \text{temp}[4] == 1)
\begin{align*}
\text{begin}
\text{out}[1] &= \text{temp}[1]; \\
\text{out}[2] &= \text{temp}[2]; \\
\text{out}[3] &= \text{temp}[3]; \\
\text{out}[4] &= \text{temp}[4]; \\
\text{out}[5] &= \text{temp}[5]; \\
\text{out}[6] &= \text{temp}[6]; \\
\text{out}[7] &= \text{temp}[7]; \\
\text{out}[8] &= \text{temp}[8];
\end{align*}
\text{end}
\text{else}
\begin{align*}
\text{out}[1:8] &= 8'b \text{00000000};
\end{align*}
\]
\[
\text{if}(a==9)
\begin{align*}
\text{begin}
\text{flag1} &= 0; \\
\text{flag} &= 0; \\
a &= 1;
\end{align*}
\text{end}
\text{count} = 0;
\]
\[
\text{end}
\]
\[
\text{count} = \text{count}+1;
\text{if}(\text{count} >156)
\text{count} = 0;
\]
\[
\text{end}
\text{else}
\begin{align*}
\text{begin}
\text{out}[1:8] &= 8'b \text{00000000};
\end{align*}
\]
Design and Implementation of FPGA based IR Encoder and Decoder compatible with TSOP 38.

end
endmodule

// Decoder .ucf

NET "clk"  LOC = "p76"  ;
NET "ena"  LOC = "p141"  ;
NET "out[1]"  LOC = "p161"  ;
NET "out[2]"  LOC = "p172"  ;
NET "out[3]"  LOC = "p156"  ;
NET "out[4]"  LOC = "p171"  ;
NET "out[5]"  LOC = "p155"  ;
NET "out[6]"  LOC = "p169"  ;
NET "out[7]"  LOC = "p154"  ;
NET "out[8]"  LOC = "p168"  ;
NET "in"  LOC = "p108"  ;

6. REFERENCES

2. Datasheets – Vishay TSOP38, Encoder HT12E, Decoder HT12D, Spartan3
3. IR transmission and reception, EL103 BEC, DAIICT