The objective of this exercise is to design an electronic lock with the following specification:

* The key is three, 4-bit numbers
  - Enter button is to be pressed between each number
  - If correct "unlocked" LED lights
  - If error, "error" LED lights after all the numbers have been entered
  - RESET button (synchronous) to start again

* When lock is open, it can be programmed
  - "Program" button; then three numbers separated by enter
  - "RESET" locks during program mode

"Enter" button when not in program mode locks.

Before you run this on FPGA, WRITE A COMPREHENSIVE TEST BENCH.